Flip-chip bonded Si Schottky diode sampling circuits for high speed demultiplexers

Jung Han Choi, Claus-Joerg Weiske†, Gerhard R. Olbrich, Peter Russer

Munich University of Technology, Arcisstr. 21, 80333 Munich, Germany

† Information and Communication Networks, Siemens AG., Hofmannstr. 51, 81359 Munich, Germany

Abstract — **This paper presents a Si Schottky diode sampling circuit for demultiplexer using flip-chip technology on alumina substrate (Al_2O_3). In order to design circuits, very high speed Si Schottky diodes, having cutoff frequency of 750 GHz, were modeled using the Root diode model and flip-chip interconnection was simulated using 3 dimensional electromagnetic simulator, HFSS.**

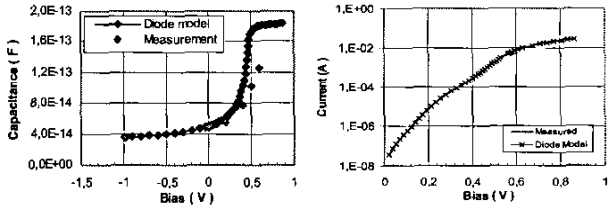
I. Introduction

Rapidly changing device technologies lead to high speed, and high performance digital circuit implementations. So far in the optical communication fields, 40 Gb/s electrical time division multiplexing (ETDM) was successfully demonstrated using InP, SiGe device technologies. Most of digital logic circuits, e.g. multiplexer and demultiplexer, were built using transistor logic cells (bipolar or HEMT). For the future development, faster switching devices are required, especially in electronic transmitter and receiver circuits for broad-band fiber-optic transmission links. However, improving device speed performance needs smaller gate length in HEMTs, smaller transit time in HBTs, and much lower parasitic components. Even modern E-beam technology and photo lithography method suffer from difficulties to reduce device channel length and to guarantee high reproducibility and yield. Hence, new conceptual design approaches are demanding. Using Schottky diodes could be a promising concept due to its high cutoff frequency above 1 THz [1]-[2]. In [2], a sampling concept in the demultiplexer circuits was demonstrated deploying diode nonlinear-transmission line (NLTL), which consists of lots of GaAs diodes and generates high amplitude strobe pulse to switch Schottky diodes sampling bridges.

In this paper, we describe the design, the fabrication, and the experimental investigation of Si Schottky diodes demultiplexer circuits. Due to the advanced Si technology, very high speed Si Schottky diodes above 700 GHz are available and were used in this circuit. Flip-chip technology was employed for the interconnection between diodes and alumina substrate, and parasitics were evaluated comparing simulation results with measurements.

II. Silicon Schottky Diode Modeling with Flip-chip Interconnections

Schottky diodes are majority carrier devices, and as a consequence, storage time due to minority carriers is quite small. Thus, Schottky diodes are challenging devices for fast switching operations. For the precise prediction of circuits employing this diode, the Root-diode model was chosen for modeling, where current and charge constitution relations decide the capacitance and conductance at each port [3]. Using Agilent's parameter extraction software, IC-CAP, the intrinsic Si diodes were modeled, excluding RF probe parasitic resistances and de-embedding open and short pattern parasitics. Fig. 1 shows the DC and CV characteristics comparing measurement results with modeling data. The DC curve shows excellent agreements between them, and the CV comparison looks quite good below the forward bias of 0.4 V. The modeled diode ideality factor, n_f, was 1.57, and the capacitance at zero bias, C_0, was approximately 50 fF.



(a) (b)

Fig. 1. Simulation of Root-diode model compared with measurements result of (a) CV characteristics and (b) DC characteristics.

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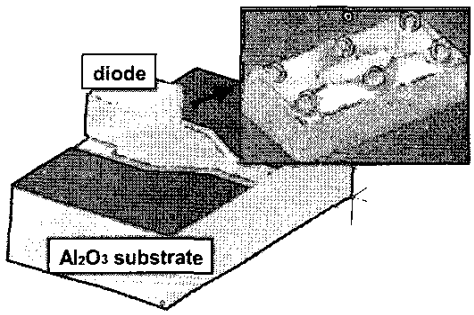
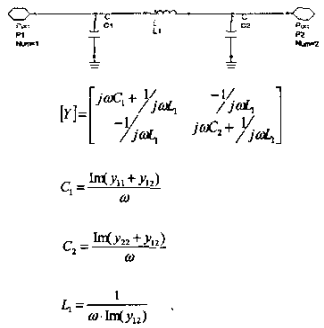
Incorporating the device model into the circuit design, the flip-chip modeling is mandatory at high frequency operating region. A 3-dimensional electromagnetic simulator, Ansoft HFSS, was utilized for circuit modeling. The actual 3-dimensional simulation structure is shown in Fig. 2(a). The Si diode was thermally compressed at 330°C to the back-side grounded alumina substrate. Bump height after bonding was measured about 5 μm. The used ideal chips are two Schottky diodes connected in series, as shown in the inset of Fig. 2(a). Each bump is made up of AuSn, and has a height of about 25 μm. Coplanar waveguide lines (CPW) with tapering structure were patterned on the substrate in order to evaluate the diode and flip-chip modeling. For the flip-chip interconnection modeling, the π-equivalent circuit was used, in Fig. 2(b) [4]. Carrying out the S-parameter simulation for the aforementioned structure and de-embedding CPW line length, which is extended for the measurement purpose, the y-parameter can be obtained.

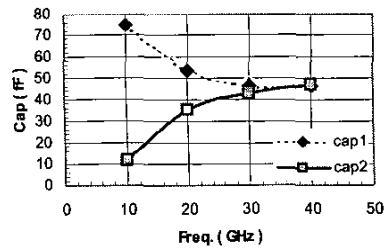


(a)

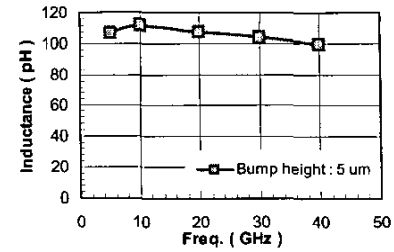


(b)

Fig. 2. (a) 3 dimensional simulation structure (b) equivalent π-circuit of flip-chip interconnection



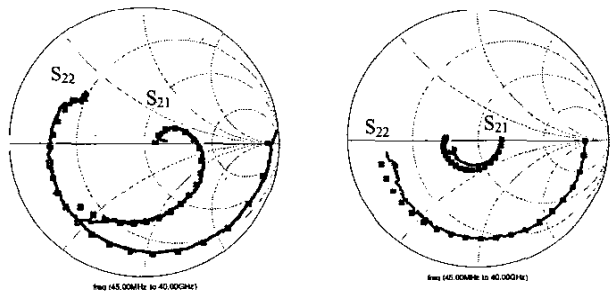
(a)



(b)

Fig. 3. (a) The simulated capacitance value and (b) inductance value of the flip-chip interconnection when the bump height is 5 μm.

Inductance and capacitance values can be calculated using equations, shown in Fig. 2(b). In Fig. 3, the calculated results are given shown varying the simulation frequency. For the simulation purpose, the average value till 40 GHz was used. C_1 is 49 fF, C_2 is 42 fF, and L_1 is 103 pF. C_1 and C_2 converge as the frequency increases till 40 GHz, whereas
the inductance L_1 remains almost same for the whole simulation frequency region. For the verification purpose,



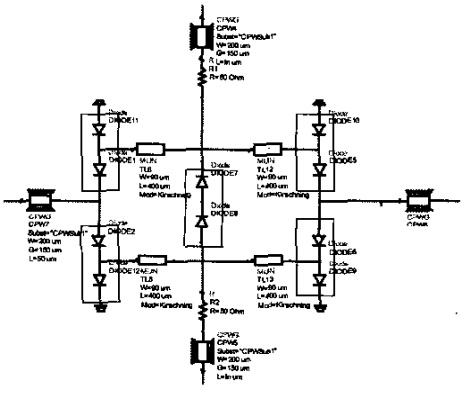
(a) $V_{forward}$ = 0.3 V (b) $V_{forward}$ = 0.7 V

Fig. 4. Measured (--) and simulated (x) s-parameters for flip-chip diodes

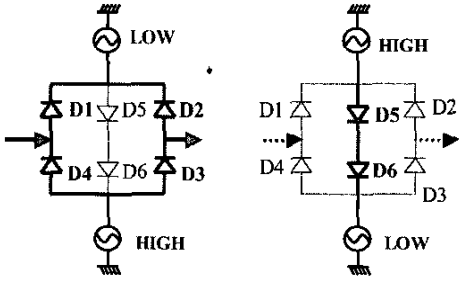
the comparison of measurement with simulation results were shown in Fig. 4. Good agreements between the measured and simulation data assured the exact modeling of the Si Schottky diodes and the flip-chip modeling up to 40 GHz.

III. Sampling Circuit Design

With the developed diode model, the diode sampling circuits were designed, as shown in Fig. 5(a). Its operation mode was depicted in Fig. 5(b), depending on the oscillation signal polarities. Reported sampling circuits composed of Schottky diodes need high amplitude strobe pulses to drive diode sampling bridge circuits [2]. Those signals were generated by a nonlinear transmission line, which is a periodically loaded line by reverse biased Schottky diodes. However, the proposed sampling bridge circuits utilize signals from the conventional oscillator.



(a)



(b)

Fig. 5. (a) The designed sampling bridge circuit schematic (b) The simplified operation modes of the bridge circuit. In the first picture, D1, D2, D3, and D4 are conducting, whereas D5 and D6 are turned off. In the second picture, vice versa.

Namely, two sinusoidal oscillator signals, which are out of phase each other and synchronized with the input signals, drive the sampling circuits. Hence, when the input signal, in which channel informations are multiplexed in time domain, is incident on the diode sampling circuit, this circuit samples the channel signal corresponding to the oscillator signal polarity.

At the sampling instant, two oscillator signals turn the sampling bridge on, then the input signal has the way to be transferred to the output port. Otherwise, all signals are reflected. Thus, 50 Ω was connected to input port in order not to deteriorate the incident signals. Five series connected Si Schottky diodes were used in the sampling bridge circuit. Four pairs of diodes (D1, D2, D3, and D4) are aligned in the same direction, forming a signal conducting path from input to output when the sampling event occurs. One pair of diodes (D5 and D6) counteract with the others when the oscillator signals are out of phase compared to the previous state. The oscillation signals are quite less reflected due to this diode pair.

IV. Simulation and Measurements

For the analysis of the circuit, a random binary signal sequence was generated, and plugged into the Agilent's RF simulation tool, Advanced Design System (ADS). The developed diode model and the flip-chip equivalent circuit parameters were considered in the simulation, so as to predict circuit behavior exactly. The simulation schematic and the results were shown in Fig. 7(a) and (b), respectively. The simulated waveform shows the demultiplexed channel signal, peaking the voltage waveform. In the simulation, two sampling circuits were simultaneously analyzed, varying the oscillator signal phase. Those circuits correspond to the demultiplexed channel each other.

The sampling circuits were fabricated using 10 mil Al_2O_3 substrate. A fabricated module is shown in Fig. 6.

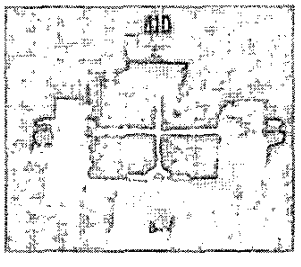
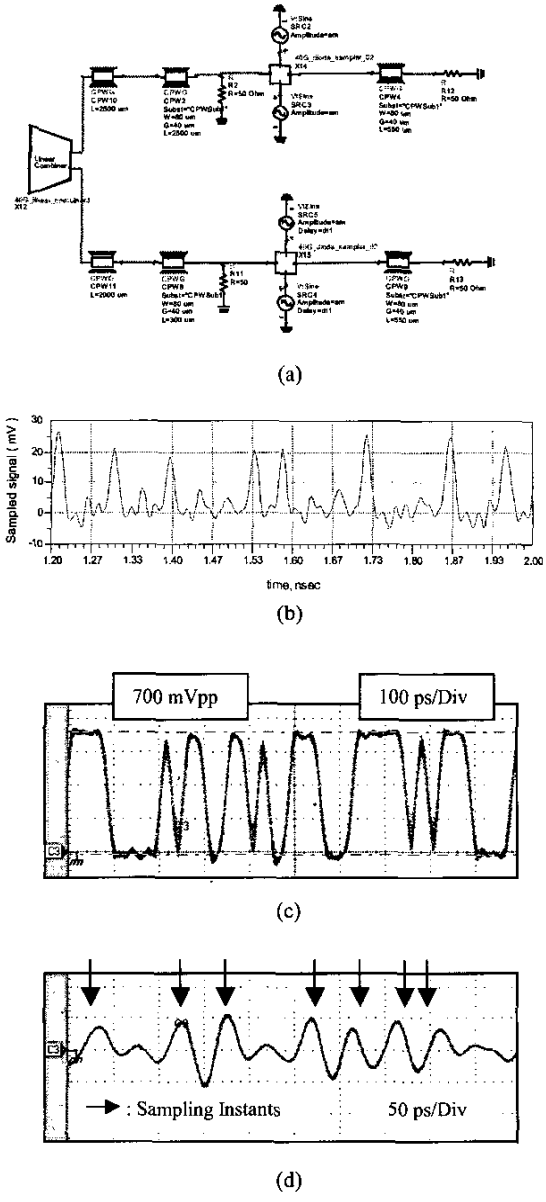


Fig. 6. The fabricated sampling bridge circuit module

The circuits included bias line to control and tune the output waveform.

In the experiment, an Anritsu pulse pattern generator (MP1763B) and a 43 Gb/s multiplexer made at Siemens were used to generate pseudo random binary sequence (PRBS) pattern. In order to synchronize the input signal with the oscillator signal, two variable delay lines were attached to the oscillator input port of the sampling circuit. The multiplexed input signal was 700 mVpp, and 42 Gb/s, which is shown in Fig. 7(c). Fig. 7(d) is the measured waveform using a digital sampling oscilloscope (Tektronix 8000). The sampling instants were dictated by arrows. Comparing simulation results, the sampling function was successfully demonstrated. The voltage ringing phenomena in the output waveform was observed. Based on the simulation analysis, the voltage ringing phenomena was dependent on the bit pattern, which is a deterministic phenomena. Therefore, employing an adaptive signal processing method, the ringing phenomena could be considerably reduced, e.g. tapped delay line filter[5].



(a) (b) (c) (d)

Fig. 7. (a) Simulation schematic (b) Sampling circuit simulation result (c) Input signal (42 Gb/s) waveform (d) Measured waveform, indicating sampling instants with arrow.

V. Conclusion

In order to construct the high speed demultiplexer digital circuits using the Si Schottky diodes, we demonstrated a Si Schottky diode sampling circuit using flip-chip technology. We established a Root diode model, and analyzed the flip-chip interconnections from the results of 3-D electromagnetic simulation. The measurements and the simulation results for the sampling circuit showed good agreement up to 40 GHz.

Acknowledgment

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